Fundamentals of Power Management for VLSI – A short course
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Summary:
Developing power management solutions for VLSI systems and mixed-signal analog/RF System-on-Chip (SoC) requires engineers with solid background in both traditional power electronics design as well as analog/RF mixed-signal VLSI design. Power management circuits with such a VLSI and SoC focus are neither covered in graduate/undergraduate power electronics courses, nor in VLSI courses. With the growing demand in the semiconductor industry for expertise in this area, there is a serious shortage in formally-trained engineers who have the necessary background combination to design efficient and cost-effective solutions for such applications. This 5-day course introduces the fundamental principles of power management system and circuit design in VLSI systems. This includes: power delivery schemes and performance metrics/characterization of power converters; linear and low-drop-out regulators; on-chip linear regulators; buck converters; loss mechanisms, modelling, and estimation; stability analysis, compensation techniques, and control schemes of linear regulators and buck converters; switching noise mitigation techniques and design considerations for mixed-signal/RF SoCs; overview of practical implementations in commercial products. The course includes design projects to exercise the knowledge acquired in an actual design.

Learning Objectives:
Upon completing the course, the participant will be able to:
• Understand power delivery schemes in VLSI systems.
• Understand power conversion/regulation system and circuit specifications and performance metrics.
• Understand circuit topologies, stability analysis, compensation techniques, control schemes, and design procedures of linear regulators and buck converters.
• Understand loss mechanisms, modelling, and estimation in switching power converters.
• Develop a comprehensive understanding of switching noise and voltage ripple mitigation techniques in switching power converters.
• Understand performance tradeoffs and the special requirements for large mixed-signal SoCs.
• Perform a transistor-level design and simulation of a linear regulator and/or a buck converter.

Target Audience:
Analog and mixed-signal designers interested in understanding the principles of power management. Product, test, system, and application engineers involved with power management characterization and testing. Design engineers interested in power management in nanometer CMOS, and integration with mixed-signal SoCs. Researchers and graduate/undergraduate students interested in power management design. RFIC design engineers will find this course helpful in understanding issues related to powering RF circuits. Technical managers will also learn current technology limitations and future technology trends.

Outline:
Day One – System level concepts, performance metrics, linear regulators
Basic definitions, Power management tasks, Schemes and challenges in mixed-signal SoCs, Types of loads, Performance metrics of voltage regulators (power management language): DC, small-signal AC, and large-signal transient metrics, Regulation Concepts, Basic linear regulator design, stability analysis and compensation.
Day Two – Linear Regulators and Buck Converters
Continuation of basic linear regulator design, PMOS versus NMOS power FETs, on-chip versus off-chip output capacitors. Basic switching power concepts, Step-down switching regulator (Buck), basic design equations, continuous and discontinuous conduction modes, loss mechanisms in switching regulators.

Day Three – Buck Converters
Control Techniques (pulse width and pulse frequency modulation), AC and small-signal modeling, stability and compensation techniques, current-mode control, hysteretic and gated-oscillator control.

Day Four – Buck Converters and Switching Noise Mitigation Techniques
Implementation examples and performance review of buck converters. Switching noise mitigation techniques: Active ripple cancellation, multi-phase converters, delta-sigma control, frequency hopping/stepping, and spur-free switching.

Day Five – Design Projects
Two transistor-level design projects will be assigned to the participants to implement and simulate under the supervision of the instructor. The projects will be the design of a buck converter or a linear regulator in a standard CMOS technology. Detailed design procedure/steps will be provided to the participants as part of the course notes. Advanced participants may choose to implement both projects if time allows. The projects require that the participants have access (through VNC or a similar tool) to a Linux workstation with a Cadence toolset and a pdk for a standard CMOS technology; all must be provided by the employer. Participants are recommended to set up a Cadence database/library for conducting the projects ahead of the project day. Participants who are not interested in or familiar with transistor-level design are not required to attend the projects day, but will find it useful to attend as discussions during that day offer additional insights into the theoretical discussions from prior days.

Ayman Fayed received his B.Sc. degree in Electronics & Communications Engineering from Cairo University in 1998, and his M.Sc. and Ph.D. degrees in Electrical & Computer Engineering from The Ohio State University in 2000 and 2004 respectively. From 2000 to 2009, he held several technical positions in the area of analog and mixed-signal design at Texas Instruments Inc., where he contributed to many product lines for wire-line, wireless, and multi-media devices. From 2000 to 2005, he was with the Connectivity Solutions Dept. at TI, where he worked on the analog frontend design of high-speed wire-line transceivers such as USB, IEEE1394b, and HDMI, and on fully integrated switching/linear regulators and battery chargers for portable media players. From 2005 to 2009, he was a member of the technical staff with the wireless analog technology center at TI, where he worked on delta-sigma data converters for various wireless standards, and on the development of fully-integrated power management solutions for mixed-signal SoCs with multi-RF cores in nanometer CMOS. Dr. Fayed joined the Dept. of Electrical & Computer Engineering at Iowa State University in 2009, where he held the Northrop Grumman Assistant Professorship. He then joined the Dept. of Electrical & Computer Engineering at The Ohio State University in 2015 as an associate professor. He is the founder and director of the Power Management Research Lab (PMRL) and his current research interests include on-chip power grids for dynamic energy distribution in highly-integrated systems, high-frequency switching regulators with on-chip and on-package passives for SoCs, low-noise power supply modulators for RF transmitters, energy-harvesting platforms for power-restricted & remotely-deployed systems, and power conversion in emerging technologies. Dr. Fayed is a senior member of IEEE, an associate editor for IEEE TCAS-I and TCAS-II, and serves in the technical program committee of RFIC, ISCAS, and the steering committee of MWSCAS. He is the author/co-author of many publications in the field and holds 10 US patents. Dr. Fayed is a recipient of NSF CAREER Award in 2013, and the 2015 Darlington Best Transactions Paper Award from the IEEE Circuits and System Society.

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